WHAT IS CLAIMED IS:

1. A magnetic memory device comprising:

a memory cell portion;

a peripheral circuit portion positioned in the vicinity of the memory cell portion;

a plurality of first magnetoresistive effect elements which are arranged in the memory cell portion and function as memory elements; and

a plurality of second magnetoresistive effect elements which are arranged in at least a part of the peripheral circuit portion and function as dummies,

wherein a sum total of occupying areas of the second magnetoresistive effect elements is 5% to 80% of the peripheral circuit portion.

2. The magnetic memory device according to claim 1, wherein an occupying area of one of the second magnetoresistive effect elements is approximately equal to that of one of the first magnetoresistive effect elements.

3. The magnetic memory device according to claim 1, wherein at least one end of each of the second magnetoresistive effect elements is electrically insulated or connected to only one end of a metal layer, and

the other end of the metal layer is electrically insulated from another metal layer.

4. The magnetic memory device according to

claim 1, wherein the memory cell portion comprises:

a first metal layer;

a second metal layer arranged to be separated from the first metal layer; and

one of the first magnetoresistive effect elements which is arranged in the vicinity of an intersection of the first and second metal layers and connected to the first and second metal layers, and

the peripheral circuit portion comprises:

a fourth metal layer which is arranged on the same surface as the first metal layer or the second metal layer; and

one of the second magnetoresistive effect elements which is arranged on the same surface as the one of the first magnetoresistive effect elements and connected to the fourth metal layer.

5. The magnetic memory device according to claim 1, wherein the memory cell portion comprises:

a first metal layer;

a second metal layer arranged to be separated from the first metal layer;

one of the first magnetoresistive effect elements which is arranged in the vicinity of an intersection of the first and second metal layers and has one end connected to the first metal layer;

a third metal layer has one end connected to the other end of the one of the first magnetoresistive

effect elements; and

a first contact layer connected to the other end of the third metal layer, and

the peripheral circuit portion comprises:

a fourth metal layer which is arranged on the same surface as the first metal layer;

a fifth metal layer which is arranged on the same surface as the second metal layer to be separated from the fourth metal layer;

one of the second magnetoresistive effect elements which is arranged on the same surface as the one of the first magnetoresistive effect elements, and has one end connected to the fourth metal layer or contacted to the same through an insulating layer;

a sixth metal layer has one end connected to the other end of the one of the second magnetoresistive effect elements and the other end is electrically insulated from another metal layer; and

a second contact layer which is connected to the fourth metal layer.

6. The magnetic memory device according to claim 5, wherein the third metal layer and the sixth metal layer are arranged on the same surface.

7. The magnetic memory device according to claim 5, wherein a plane shape of the sixth metal layer is approximately the same as a plane shape of the one of the second magnetoresistive effect elements.

8. The magnetic memory device according to claim 5, wherein the one of the second magnetoresistive effect elements is arranged in an area other than an intersection of the fourth and fifth metal layers.

9. The magnetic memory device according to claim 5, wherein the memory cell portion further includes a first cap layer arranged between the one of the first magnetoresistive effect elements and the first metal layer, and

the peripheral circuit portion further includes a second cap layer arranged between the one of the second magnetoresistive effect elements and the fourth metal layer.

10. The magnetic memory device according to claim 9, wherein a plane shape of the first cap layer is approximately the same as a plane shape of the one of the first magnetoresistive effect elements, and a plane shape of the second cap layer is approximately the same as a plane shape of the one of the second magnetoresistive effect elements.

11. A magnetic memory device comprising:

a memory cell portion;

a peripheral circuit portion positioned in the vicinity of the memory cell portion;

a plurality of first magnetoresistive effect elements which are arranged in the memory cell portion and function as memory elements; and

a plurality of second magnetoresistive effect elements which are arranged in the entire peripheral circuit portion and function as dummies,

wherein a sum total of occupying areas of the second magnetoresistive effect elements is 5% to 80% of a predetermined area arbitrarily selected from the peripheral circuit portion.

12. The magnetic memory device according to claim 11, wherein an occupying area of one of the second magnetoresistive effect elements is approximately equal to that of one of the first magnetoresistive effect elements.

13. The magnetic memory device according to claim 11, wherein a size of the predetermined area is tenfold of one cell.

14. The magnetic memory device according to claim 11, wherein a size of the predetermined area corresponds to a regular tetragon in which each side is 0.1 mm.

15. The magnetic memory device according to claim 11, wherein a shape of the predetermined area is an isotropic shape.

16. The magnetic memory device according to claim 11, wherein at least one end of each of the second magnetoresistive effect elements is electrically insulated or connected to only one end of a metal layer, and

the other end of the metal layer is electrically insulated from another metal layer.

17. The magnetic memory device according to claim 11, wherein the memory cell portion comprises:

a first metal layer;

a second metal layer arranged to be separated from the first metal layer; and

one of the first magnetoresistive effect elements which is arranged in the vicinity of an intersection of the first and second metal layers and connected to the first and second metal layers, and

the peripheral circuit portion comprises:

a fourth metal layer which is arranged on the same surface as the first metal layer or the second metal layer; and

one of the second magnetoresistive effect elements which is arranged on the same surface as the one of the first magnetoresistive effect elements and connected to the fourth metal layer.

18. The magnetic memory device according to claim 11, wherein the memory cell portion comprises:

a first metal layer;

a second metal layer arranged to be separated from the first metal layer;

one of the first magnetoresistive effect elements which is arranged in the vicinity of an intersection of the first and second metal layers and has one end

connected to the first metal layer;

a third metal layer has one end connected to the other end of the one of the first magnetoresistive effect elements; and

a first contact layer connected to the other end of the third metal layer, and

the peripheral circuit portion comprises:

a fourth metal layer which is arranged on the same surface as the first metal layer;

a fifth metal layer which is arranged on the same surface as the second metal layer to be separated from the fourth metal layer;

one of the second magnetoresistive effect elements which is arranged on the same surface as the one of the first magnetoresistive effect elements, and has one end connected to the fourth metal layer or contacted to the same through an insulating layer;

a sixth metal layer has one end connected to the other end of the one of the second magnetoresistive effect elements and the other end is electrically insulated from another metal layer; and

a second contact layer which is connected to the fourth metal layer.

19. The magnetic memory device according to claim 18, wherein the third metal layer and the sixth metal layer are arranged on the same surface.

20. The magnetic memory device according to

claim 18, wherein a plane shape of the sixth metal layer is approximately the same as a plane shape of the one of the second magnetoresistive effect elements.

21. The magnetic memory device according to claim 18, wherein the one of the second magnetoresistive effect elements is arranged in an area other than an intersection of the fourth and fifth metal layers.

22. The magnetic memory device according to claim 18, wherein the memory cell portion further includes a first cap layer arranged between the one of the first magnetoresistive effect elements and the first metal layer, and

the peripheral circuit portion further includes a second cap layer arranged between the one of the second magnetoresistive effect elements and the fourth metal layer.

23. The magnetic memory device according to claim 22, wherein a plane shape of the first cap layer is approximately the same as a plane shape of the one of the first magnetoresistive effect elements, and a plane shape of the second cap layer is approximately the same as a plane shape of the one of the second magnetoresistive effect elements.

24. A magnetic memory device comprising:

a memory cell portion;

a peripheral circuit portion positioned in the

vicinity of the memory cell portion;

a memory chip including the memory cell portion and the peripheral circuit portion;

a plurality of first magnetoresistive effect elements which are arranged in the memory cell portion and function as memory elements; and

a plurality of second magnetoresistive effect elements arranged in the entire memory chip and function as dummies,

wherein a sum total of occupying areas of the first and second magnetoresistive effect elements is 5% to 80% of a predetermined area arbitrarily selected from the memory chip.

25. A method of manufacturing a magnetic memory device having a memory cell portion and a peripheral circuit portion, comprising:

forming a first metal material film in each of the memory cell portion and the peripheral circuit portion;

forming a magnetoresistive effect film on the first metal material film in each of the memory cell portion and the peripheral circuit portion;

forming a cap film on the magnetoresistive effect film in each of the memory cell portion and the peripheral circuit portion;

forming a first cap layer by patterning the cap film of the memory cell portion into a first shape, and forming a second cap layer by patterning the cap film

of the peripheral circuit portion into a second shape;

forming a first magnetoresistive effect element which functions as a memory element by patterning the magnetoresistive effect film of the memory cell portion into the first shape by using the first cap layer, and forming a second magnetoresistive effect element which functions as a dummy by patterning the magnetoresistive effect film of the peripheral circuit portion into the second shape by using the second cap layer;

forming a first metal layer by patterning the first metal material film of the memory cell portion into a third shape, and forming a second metal layer by patterning the first metal material film of the peripheral circuit portion into a fourth shape;

forming a first insulating film on the first and second cap layers and the first and second metal layers in each of the memory cell portion and the peripheral circuit portion;

flattening the first insulating film; and

removing the first insulating film until a surface of the first cap layer is exposed.

26. The method of manufacturing a magnetic memory device according to claim 25, wherein the fourth shape is approximately the same as the second shape.

27. The method of manufacturing a magnetic memory device according to claim 25, further comprising forming a second insulating film on a exposed surface

of the second cap layer and the first insulating film only in the peripheral circuit portion.

28. The method of manufacturing a magnetic memory device according to claim 25, wherein the first and second cap layers are formed of conductive films and are used as contacts.

29. The method of manufacturing a magnetic memory device according to claim 25, further comprising:

forming a first hard mask having the first shape on the cap film in the memory cell portion;

forming a second hard mask having the second shape on the cap film in the peripheral circuit portion;

patterning the cap film by using the first and second hard masks; and

removing the first and second hard masks.

30. The method of manufacturing a magnetic memory device according to claim 29, wherein the first and second hard masks are insulating films.

31. The method of manufacturing a magnetic memory device according to claim 25, wherein a plurality of the second magnetoresistive effect elements are formed on at least a part of the peripheral circuit portion, and a sum total of occupying areas of the plurality of the second magnetoresistive effect elements is 5% to 80% of the peripheral circuit portion.

32. The method of manufacturing a magnetic memory device according to claim 31, wherein an occupying area

of the second magnetoresistive effect element is approximately equal to that of the first magnetoresistive effect element.

33. The method of manufacturing a magnetic memory device according to claim 25, wherein a plurality of the second magnetoresistive effect elements are formed on the whole of the memory cell portion, and a sum total of occupying areas of the plurality of the second magnetoresistive effect elements is 5% to 80% of a predetermined area arbitrarily selected from the peripheral circuit portion.

34. The method of manufacturing a magnetic memory device according to claim 33, wherein an occupying area of the second magnetoresistive effect element is equal to that of the first magnetoresistive effect element.

35. The method of manufacturing a magnetic memory device according to claim 25, wherein a plurality of the second magnetoresistive effect elements are formed on the entire memory chip, a sum total of occupying areas of a plurality of the first magnetoresistive effect elements and the plurality of second magnetoresistive effect elements is 5% to 80% of a predetermined area arbitrarily selected from the memory chip.